In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) An apparatus for computing the absolute value of a complex number having a real part and an imaginary part, wherein the real and imaginary parts of the complex number are each represented by a digital number of B bits, where B is an integral factor of 4, the apparatus comprising:

a first squaring unit having an input receiving said real part of said complex number and an output generating a first square of said real part multiplied with itself;

a second squaring unit having and input receiving said imaginary part of said complex number and an output generating a second of said imaginary part multiplied with itself;

said first squaring unit and said second squaring unit each include:

a first multiplier having a first input receiving a set of B/2 least significant bits of said input, a second input receiving said set of B/2 least significant bits of said input and a product output generating a first product of said B least significant bits multiplied by itself,

a second multiplier having a first input receiving a set of B/2 most significant bits of said input, a second input receiving said set of B/2 most significant bits of said input and a product output generating a second product of said B most significant bits multiplied by itself,

a third multiplier having a first input receiving said set of B/2 least significant bits of said input, a second input receiving said set of B/2 most significant bits of said input and a product output generating a third product of said

B least significant bits multiplied by said B most significant bits,

a shift unit having an input receiving said product output of said third multiplier and a shift output generating a left shifted output left shifted by (B/2)+1 bits, and

a summing unit having a first input having least significant bits receiving said first product and most significant bits receiving said second product, a second input receiving said left shifted output and generating a sum output being a sum of said first and second inputs, said sum output being said output of said squaring unit;

said first multiplier of each of said first squaring unit and said second squaring unit includes

a fourth multiplier having a tenth input receiving a set of B/4 least significant bits of said first input of said corresponding multiplier, a second input receiving said set of B/4 least significant bits of said first input of said corresponding multiplier and a product output generating a fourth product of said B/4 least significant bits multiplied by itself,

a fifth multiplier having a first input receiving a set of B/4 most significant bits of said first input of said corresponding multiplier, a second input receiving said set of B/4 most significant bits of said first input of said corresponding multiplier and a product output generating a fifth product of said B/4 most significant bits multiplied by itself,

a sixth multiplier having a first input receiving said set of B/4 least significant bits of said first input of said corresponding multiplier, a second input receiving said set of B/4 most significant bits of said first input of said corresponding multiplier and a product output generating a

sixth product of said B/4 least significant bits multiplied by said B/4 most significant bits,

a shift unit having an input receiving said output of said sixth multiplier and a shift output generating an left shifted output left shifted by (B/4)+1 bits, and

a summing unit having a first input having least significant bits receiving said third product and most significant bits receiving said fourth product, a second input receiving said left shifted output and generating a sum output being a sum of said first and second inputs, said sum output being said output of said multiplier;

a summing unit having a first input receiving said first square, having a second input receiving said second square and an output generating a sum of said first square and said second square; and

a square root unit having an input receiving said sum and an output generating a square root of said sum, said square root being said absolute value of said complex number.

2. (Canceled)

3. (Currently Amended) The apparatus of claim ~~2~~ 1, wherein the real and imaginary parts of the complex number are each represented by a signed digital number, and wherein:

said first multiplier of each of said first and second squaring units is an unsigned ~~multipliers~~ multiplier;

said second and third multipliers of each of said first and second squaring unit are ~~a~~ signed ~~multiplier~~ multipliers; and

said summing unit is a signed summing unit.

4 to 8. (Canceled)

9. (Currently Amended) ~~The~~ An apparatus ~~of claim 1, wherein~~ for computing the absolute value of a complex number having a real part and an imaginary part, the apparatus comprising:

a first squaring unit having an input receiving said real part of said complex number and an output generating a first square of said real part multiplied with itself;

a second squaring unit having and input receiving said imaginary part of said complex number and an output generating a second of said imaginary part multiplied with itself;

a summing unit having a first input receiving said first square, having a second input receiving said second square and an output generating a sum of said first square and said second square; and

a square root unit having an input receiving said sum and an output generating a square root of said sum, said square root being said absolute value of said complex number, said square root unit ~~includes~~ including a plurality of processing elements equal in number to a number of bits representing said real part and said imaginary part of said complex number disposed in a cascade chain, each processing element having

a current data input, said current data input of a first processing element in said chain receiving said sum output of said summing unit,

a current remainder input, said current remainder input of said first processing element in said chain receiving a zero input,

a current root input, said current root input of said first processing element in said chain receiving a zero input,

a next data output, said next data output connected to said current data input of a next processing element in said chain,

a next remainder output, said next remainder output connected to said current remainder input of a next processing element in said chain, said next remainder output of a last processing element in said chain forming a remainder part of said square root,

a next root output, said next root output connected to said current root input of a next processing element in said chain, said next root output of said last processing element in said chain forming an integer part of said square root,

a shift unit having an input connected to said current data input and an output connected to said next data output, said shift unit left shifting said current data input two bits,

a signed summing unit having a positive input receiving as least significant bits two most significant bits of said current data input and bits of said current remainder input left shifted two bits and a negative input having two least significant bits receiving the digital constant "01" and bits receiving said current root input left shifted two bits, said signed summing unit generating a difference output corresponding to a difference of said positive input minus said negative input and a sign bit indicating a sign of said difference,

a first multiplexer having a first input receiving as least significant bits two most significant bits of said current data input and bits of said current remainder input left shifted two bits, a second input receiving said difference output, a control input receiving said sign bit and an output coupling a selected one of said first input and said second input dependent upon said control input, said output connected to said next remainder output, and

a second multiplexer having a first input receiving as least significant bit a digital constant "0" and bits of said current root input left shifted one bit, a second input receiving as least significant bit a digital constant "1" and bits of said current root input left shifted one bit, a control input receiving said sign bit and an output coupling a selected one of said first input and said second input dependent upon said control input, said output connected to said next root output.

10. (Original) The apparatus of claim 9, wherein:
each processing element further having
a first data latch having an input receiving said shift unit output temporarily storing said next data output,
a second data latch having an input receiving said output of said first multiplexer temporarily storing said next remainder output, and
a third data latch having an input receiving said output of said second multiplexer temporarily storing said next root output.

11. (Original) The apparatus of claim 9, wherein:
said square root unit includes
at least one processing element disposed in a cascade chain, each processing element having
a current data input, said current data input of a first processing element in said chain receiving said sum output of said summing unit,
a current remainder input, said current remainder input of said first processing element in said chain receiving a zero input,

a current root input, said current root input of said first processing element in said chain receiving a zero input,

a next data output, said next data output connected to said current data input of a next processing element in said chain,

a next remainder output, said next remainder output connected to said current remainder input of a next processing element in said chain,

a next root output, said next root output connected to said current root input of a next processing element in said chain,

a shift unit having an input connected to said current data input and an output connected to said next data output, said shift unit left shifting said current data input two bits,

a signed summing unit having a positive input receiving as least significant bits two most significant bits of said current data input and bits of said current remainder input left shifted two bits and a negative input having two least significant bits receiving the digital constant "01" and bits receiving said current root input left shifted two bits, said signed summing unit generating a difference output corresponding to a difference of said positive input minus said negative input and a sign bit indicating a sign of said difference,

a first multiplexer having a first input receiving as least significant bits two most significant bits of said current data input and bits of said current remainder input left shifted two bits, a second input receiving said difference output, a control input

receiving said sign bit and an output coupling a selected one of said first input and said second input dependent upon said control input, said output connected to said next remainder output, and

a second multiplexer having a first input receiving as least significant bit a digital constant "0" and bits of said current root input left shifted one bit, a second input receiving as least significant bit a digital constant "1" and bits of said current root input left shifted one bit, a control input receiving said sign bit and an output coupling a selected one of said first input and said second input dependent upon said control input, said output connected to said next root output;

a switch having

a first data input receiving said sum output of said summing unit,

a second data input receiving said next data output of a last processing element in said chain,

a remainder input receiving said next remainder output of said last processing element in said chain,

a root input receiving said next root output of said last processing element in said chain,

a data output connected to said current data input of a first processing element in said chain,

a first remainder output connected to said current remainder input of said first processing element in said chain,

a first root output connected to said current root of said first processing element in said chain,

a second remainder output a remainder part of said square root, and

a second root output forming an integer part of said square root,

said switch having a first state connecting said first input data to said data output, a digital constant "0" to said first remainder output, a digital constant "0" to said first root output and said root input to said second root output,

said switch having a second state connecting said second data input to said data output, said remainder input to said first remainder output and said root input to said first root output; and

a loop control connected to said switch, said loop control controlling said first and second states of said switch to input data to said chain of processing elements, recirculate said data, remainder and root from said last processing element in said chain to said first processing element in said chain at least once, and output a calculated root.

12. (Original) The apparatus of claim 11, wherein:

said first state of said switch further connects said remainder input to said remainder output.

13. (Original) The apparatus of claim 11, wherein:

each processing element further having

a first data latch having an input receiving said shift unit output temporarily storing said next data output,

a second data latch having an input receiving said output of said first multiplexer temporarily storing said next remainder output, and

a third data latch having an input receiving said output of said second multiplexer temporarily storing said next root output.